DESIGN AND FABRICATION OF ELECTRO-THERMAL MICROCANTILEVERS FOR ULTRAFAST MOLECULAR SORTING AND DELIVERY

BY

NICHOLAS I. MANISCALCO

THESIS

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Adviser:

Associate Professor William P. King

ABSTRACT

Improvements to the current state of the art in microfabricated cantilevers are investigated in order to realize enhanced functionality and increased versatility for use in ultrafast electrophoretic molecular sorting and delivery. Design rationale and fabrication process flow are described for six types of electro-thermal microcantilevers. Devices have been tailored for the process of separating mixtures of heterogeneous molecules into discrete detectable bands based on electrophoretic mobility, and delivering them to a conductive substrate using electric fields. Four device types include integrated heating elements capable of warming samples to catalyze reactions or cleaning the device for reuse. Similar devices have been shown to be capable of targeting temperatures between ambient conditions and the melting point of silicon, to within 0.1˚C precision or better[1]. All microcantilevers types are equipped with a highly doped conductive silicon tip capable of interacting with a conductive substrate to deliver molecules under the presence of an electric field. Devices are equipped with additional electrodes to aid in sorting molecules on the surface of the probe end. Two designs contain two legs and one additional sorting electrode while four designs contain three legs and have two sorting electrodes. Devices having two sorting electrodes are designed to be capable of sorting three or more molecular species, a distinctive advancement in the state of the art. A detailed process flow of the fabrication process for all six electro-thermal cantilever designs are explained in detail.

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CHAPTER 1

INTRODUCTION

Atomic force microscopy (AFM) microcantilevers have matured into versatile tools capable of characterizing materials with nanometer resolution.[2-4] AFM has recently been demonstrated to be useful in performing ultrafast electrophoretic differentiation of molecules on populations of <0.1 zeptomoles (10^{-22} moles) on the surface of a modified commercial probe tip. In this demonstration 5-mer and 16-mer single stranded DNA oligonucleotide fragments exhibit migration times approximately five orders of magnitude faster than the state of the art conventional capillary electrophoresis system. A large electric field applied over the length of an AFM tip result in enhanced differential mobilities stemming from the confinement of the water layer formed on the tip surface.[5]

Capillary electrophoresis is a powerful method with high sensitivity and selectivity used to sort molecules based on their size to charge ratios. These results were produced by coating the backside of a commercial AFM probe with a metallic coating. The tip of the probe is modified for surface adsorption compatibility by dip coating a low molecular weight silane, providing a hydrophilic surface for a 2-3nm condensed water to form upon. In contrast to bulk electrophoresis in water, this 2 nm water layer supports electro-osmotic flow which can be used to drive the motion of neutral molecules. In this experiment the tip is dip coated with a binary fluid containing the oligonucleotide fragments [Figure 1.1(a)]. The probe is brought into contact with a conductive substrate and an electric field is applied between them in order to drive the molecules toward the base of the tip [Figure 1.1(b)]. Molecules are driven down the length of the tip toward the substrate by switching the electric field polarity [Figure 1.1(c)]. If the applied pulse width

is larger than the time required for the molecules to travel the entire length of the tip, the molecules will deposit on the substrate. The total transit time for a migrating solute species depends on its electrophoretic mobility. Molecules with lower electrophoretic mobilities are driven back to the base of the tip [Figure 1.1(d)]. Precise control over the applied pulse width permits discrete molecular populations to be sorted and delivered in this fashion.

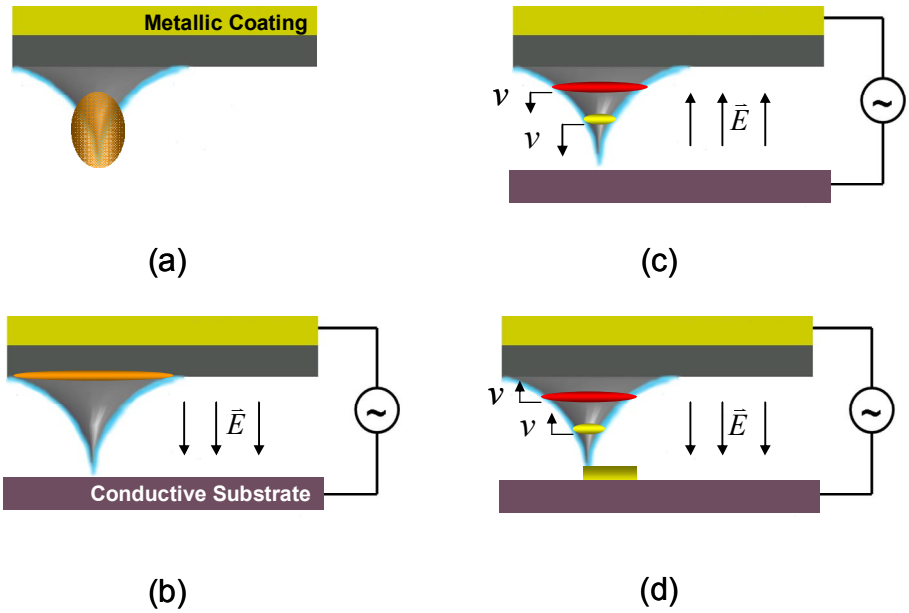


Figure 1.1 Electrophoresis on AFM. (a) Molecules are dip coated onto tip. (b) Electric field is applied, driving molecules to base of tip. (c) Molecules separate into discrete bands as they are driven toward substrate. (d) Molecules with high mobilities are deposited onto substrate, those with lower mobilities are driven back toward tip base.

Further modifications to commercially available microfabricated cantilevers are necessary to incorporate improved functionality for ultrafast molecular sorting and delivery. Advancements considered in this paper include the addition sorting electrodes and an integrated heater.

Microcantilevers with integrated heaters have been previously developed for thermomechanical data storage[6] and nano-manufacturing[7], and metrology[8]. Heaters are usually produced by selectively doping the silicon. By implanting silicon with different

impurity concentrations the number of charge carriers in regions can be controlled locally. This translates into the capability of carefully controlling resistivity and resistance. While low resistance regions readily conduct the current, high resistance regions release heat due to Joule heating phenomenon. Selectively doped silicon cantilevers have been shown to be capable of reaching temperatures as high as 900˚C within a few microseconds.[9]

CHAPTER 2

DESIGN RATIONALE

The design of microfabricated cantilevers is investigated in order to realize improved functionality and increased versatility for use in ultrafast electrophoretic molecular sorting and delivery. These device types are optimized to be capable of separating mixtures of heterogeneous molecules and deliver them to a conductive substrate in discrete detectable bands based on the molecules electrophoretic mobility using electric fields. Designs I, II, III, and V also include integrated heating elements capable of heating samples to catalyze reactions or for cleaning the device between experiments.

All microcantilevers types are equipped with a highly doped conductive silicon tip capable of interacting with a conductive substrate to deliver molecules under the presence of an electric field. The tip electrode is made electrically active by highly doping the silicon with phosphorus. Highly doped silicon was chosen as an electrode material in favor of a metal due to the practicability of modifying the tip for adsorption. To do this a silane is dip coated onto the silicon which attaches well to the native oxide that is formed silicon, producing a hydrophilic surface. This is important to device performance since the condensed water layer forming on the hydrophilic surface permits separation and delivery of neutral molecular species through electro-osmotic motion of the water.

Devices are also equipped with additional electrodes of various geometry types to assist in sorting molecules into discrete molecular bands in the presence of an electric field on the surface of the probe end. Devices I and II are equipped with one additional

sorting electrode while designs III, IV, V, and VI have two. All sorting electrodes are fabricated with platinum electrodes. Platinum is resistant to chemical attack, has excellent high-temperature characteristics, and stable electrical properties. Platinum is considered an inert electrode material due to its low reactivity with ionic solutions, it also has the advantage that under an electrical potential it is less reactive to ions in an electrolyte than other metals such as silver and gold.[10] Furthermore, platinum will not easily oxidize at any temperature as many metals do in an oxygen environment, which would have the deleterious effect of altering electrical characteristics due to probe heating.

Designs I and II are two legged devices with one highly doped silicon tip electrode and one platinum sorting electrode. The end of sorting electrode in Design I is shaped as a semicircle concave to the tip at a fixed distance of 12μm. The end of the sorting electrode in Design II has a flat end at a fixed distance of 12μm to the tip electrode. Designs III, IV, V, and VI are three legged devices with a highly doped silicon tip electrode and two platinum sorting electrodes. The sorting electrodes in Designs III and IV are shaped as parallel plates with a separation of 4μm from the tip electrode and 14μm from one another. The sorting electrodes in Designs V and VI have ends which are pointed with an apex facing the tip; these electrodes have a separation of 4μm from the tip electrode and 14μm from one another. Designs I, II, III and V are lightly doped with phosphorus to produce a heating element, while Designs IV and VI are not thermally active. All six designs can be seen in Figure 2.1, relevant physical dimensions and theoretical mechanical properties are also included in Table 2.1.

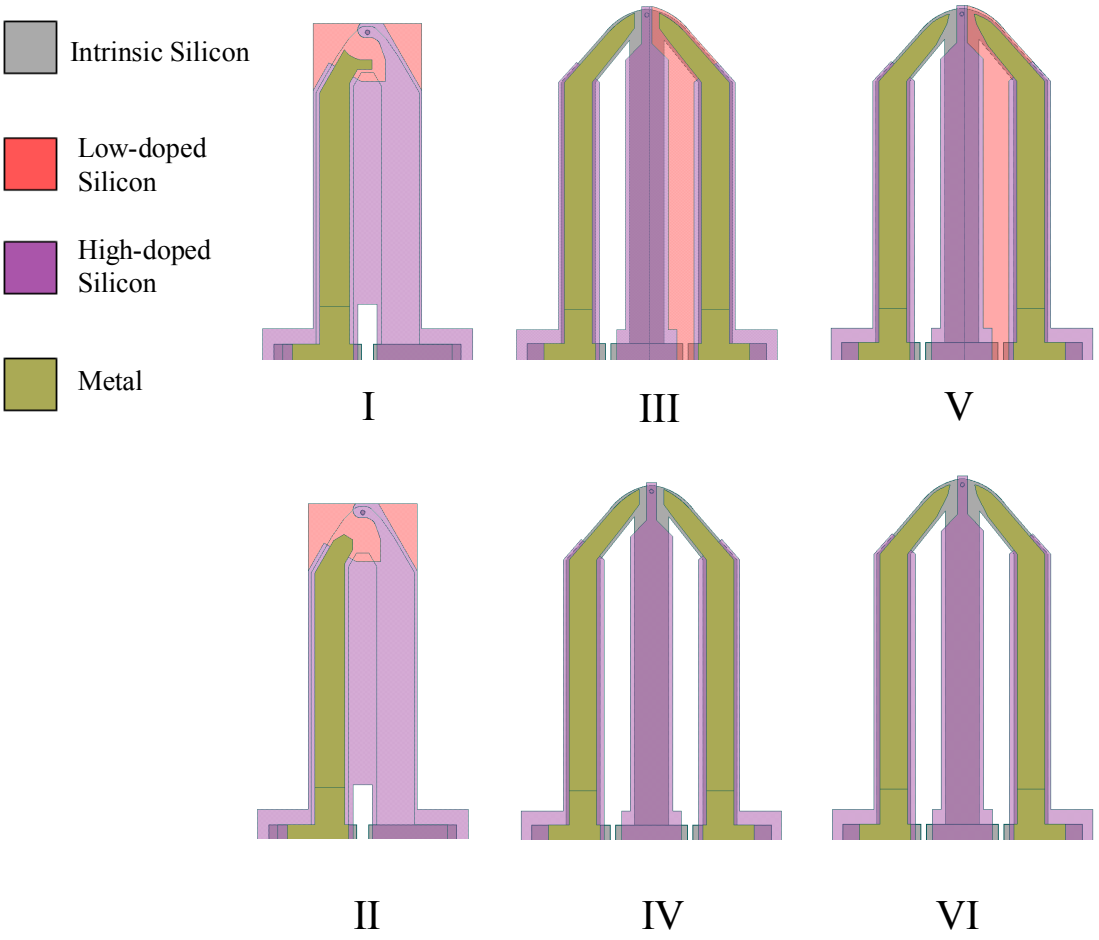


Figure 2.1. Electro-Thermal Cantilever Designs

Design	Number of Legs	Leg Width (um)	Leg Length (um)	Theoretical Spring Constant (N/m)	Sorting Electrode Spacing (um)	Heating Electrode Spacing (um)
I	2	20	165	0.33	12	12
II	2	20	165	0.33	12	12
III	3	20	195	0.30	14	4
IV	3	20	195	0.30	14	-
V	3	20	195	0.30	14	4
VI	3	20	195	0.30	14	-

Table 2.1 Physical dimensions and theoretical mechanical properties of electro-thermal cantilevers.

For the two legged designs I and II, molecules on the probe end will be separated into discrete bands based on their electrophoretic mobility when a voltage bias is placed between the tip and sorting electrode. Operating the devices in this mode will also cause

the probe to release heat as current flows through the low doped silicon region. Molecules can be delivered to the substrate by placing a voltage bias between the tip electrode and a conductive substrate.

The three legged devices with heaters, Designs III and V, can be operated in three distinct modes, molecular sorting, heating, and delivery. To sort molecules based on electrophoretic mobility a voltage bias is placed between the two sorting electrodes, labeled A and C in Figure 2.2. Fluids containing more than two molecular species can be sorted into discrete bands laterally in this manner. To heat molecules on the probe end, a voltage bias is placed between the tip electrode and sorting electrode A. This will force current to travel through highly resistive silicon, resulting in joule heating of the substrate. To deliver molecules to the conductive substrate a voltage bias is placed between the tip electrode, B, and the conductive substrate. The three legged devices without heaters, Designs IV and VI, can only be operated in sorting and delivery modes.

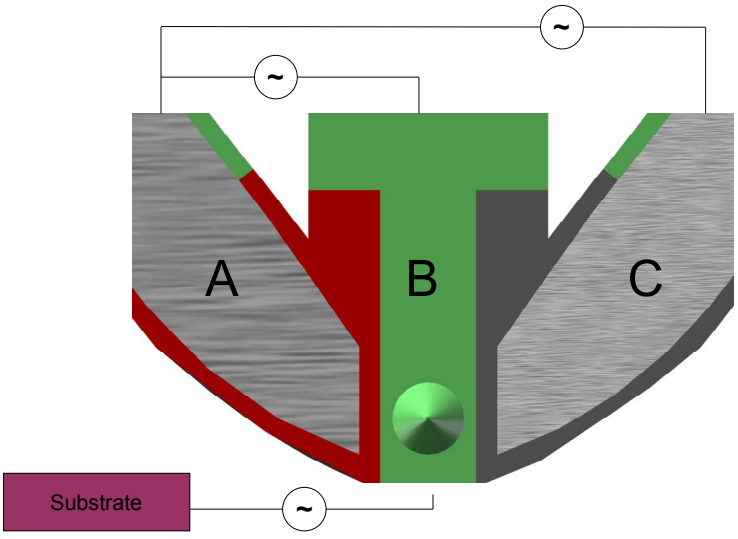


Figure 2.2 Three legged device functionality. A voltage bias is placed between the tip electrode B and a conductive substrate for molecular delivery. A voltage bias is placed between electrodes A and C to sort molecules. A voltage bias is placed between A and B to heat molecules.

CHAPTER 3

FABRICATION PROCESS

This chapter describes the fabrication of specialized electro-thermal cantilevers in detail. The device fabrication procedures are built upon an evolution of processing techniques first developed by IBM Zurich Research Laboratory groups[11]. These methods have been further progressed at Stanford University[12] and Georgia Tech[13] to produce various specialized heated AFM cantilevers. These techniques have been customized for production in the Micro-Nano-Mechanical Systems Laboratory (MNMS) and the Micro & Nanotechnology Laboratory (MNTL) facilities at the University of Illinois Urbana-Champaign. Fabrication of electro-thermal cantilevers are categorized into five major processing steps; 1) tip & anchor formation, 2) cantilever beam formation, 3) electrical activation, 4) passivation & metallization, 5) device release. The general process flow for is seen in Figure 3.1, using Design III as the model geometry.

Devices are fabricated on a 100mm (4inch) n-type phosphorus float zone (FZ) grown double side polished silicon-on-insulator (SOI) wafer with a <100> crystal orientation. The SOI wafer selected has a device layer thickness of 5μm, a buried oxide layer of 1μm, and a handle wafer thickness of 500μm. The device layer has an intrinsic resistivity of 38.3-51.7 Ω-cm. It is desirable to have a high device layer resistivity for this design in order to prevent current leakage between the electrodes during specific modes operation. For this reason float zone manufactured wafers are used since this method of growing silicon allows wafer manufacturers to achieve much higher resistivity's than possible with the conventional Czocharlski (CZ) process of growing silicon.

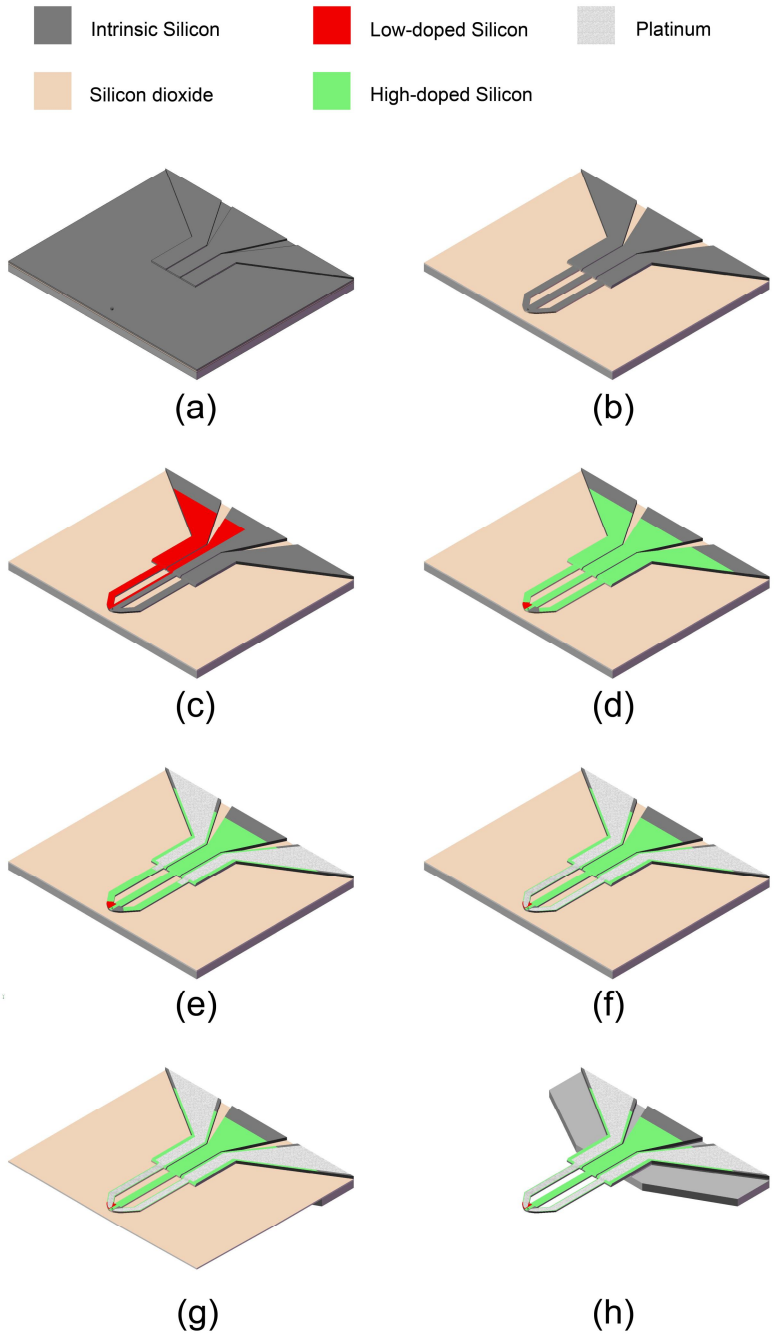
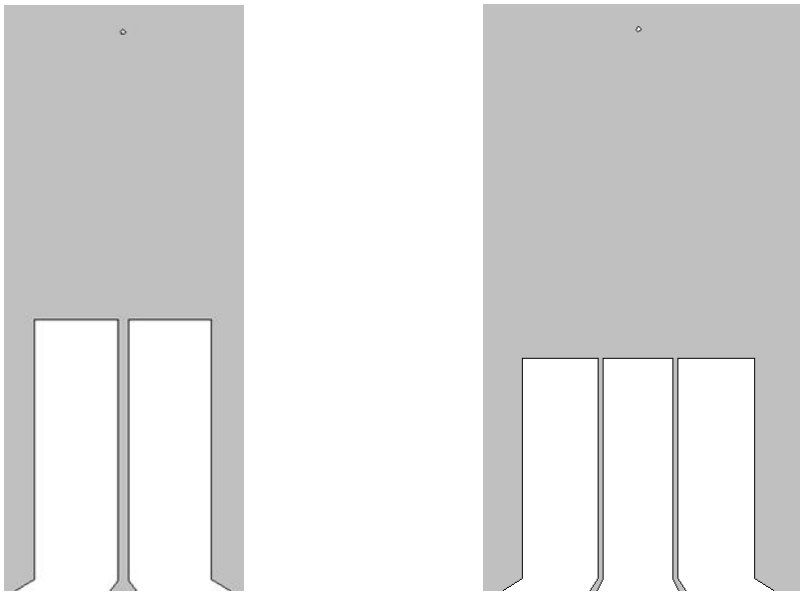


Figure 3.1 Schematic of fabrication process for all electro-thermal cantilevers. (a) Anchors and pillars are etched into the device layer. Pillars are sharpened into tips. (b)Cantilever beams are etched. (c) Devices are selectively doped with a low concentration of phosphorus to form heater region. (d) Devices are selectively doped with high concentration phosphorus to form high current carrying electrodes. (e) A thin gold film is patterned to form the contact electrodes. (f) A thin film of platinum is patterned to form beam electrodes. (g) A backside etch of the handle silicon layer is performed. The buried oxide layer is removed in a hydrofluoric bath, rendering a free standing device.

3.1 Tip & Anchor Formation

Tip formation is a three step process. First pillars are formed on the device layer, these pillars are thinned in an isotropic etch, and finally sharpened into final form via thermal oxidation. Photolithography is utilized to mask anchor regions and 2.7μm circles which define the pillar diameters. A 1.5μm thick negative photoresist, NR71-1500, is spun onto the wafer and then baked on a hotplate to allow solvents in the resist to evaporate causing the film to densify. The wafer is then loaded into a mask aligner and exposed to ultraviolet (UV) radiation. The photomask, [Figure 3.2], allows UV light to pass through transparent regions and prohibits passage of UV light in opaque regions, transferring the pattern from the mask to the resist. Areas of the negative resist exposed to radiation crosslink, rendering them less soluble in an organic solvent developer solution. Upon development unexposed regions wash away yielding the desired pattern. The photoresist is hard baked onto the wafer removing any remaining solvents to make the photoresist resistant to etching.

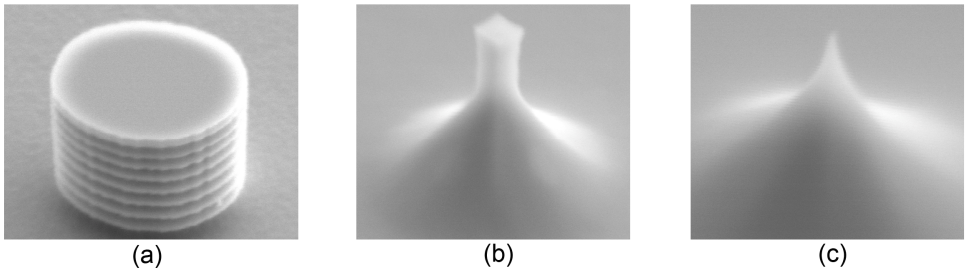
The wafer is anisotropically etched in an inductively-coupled plasma deep reactive etch (ICP-DRIE) procedure known as the Bosch process. The Bosch process allows for the creation of deep trenches with large depth to width aspect ratios[14]. This etch defines the height of anchors and pillars to ~2μm. A SEM image of a pillar is seen in Figure 3.3a. Remaining photoresist is removed by soaking the wafer in acetone and piranha solution. Piranha is a mixture of sulfuric acid (70%) and hydrogen peroxide (30%); this is performed on a hotplate at 120˚C to propel the reaction.



(a) **(b)**

Figure 3.2 Tip/Anchor Formation Mask. (a) Designs I, II (b) Designs III, IV, V, and VI. White areas represent where the tips and anchors will be formed. Shaded areas will be etched during anisotropic etching

Next pillars are thinned by submerging the wafer in an isotropic etchant consisting of hydrofluoric acid (2%), nitric acid (95%), and acetic acid (3%). This is a common isotropic etchant in micro-manufacturing often referred to as HNA. The nitric acid in the solution oxidizes the silicon forming silicon oxide which is consumed by the hydrofluoric acid in the solution. The acetic acid stabilizes this reaction[14]. The pillar diameters are thinned down to approximately, 0.5μm [Figure 3.3b].



(a) (b) (c)

Figure 3.3 Scanning Electron Microscope images of pillar/tip region throughout tip formation process. (a) Pillar formed by Bosch process. (b) Image of pillar following isotropic etch used to thin pillars. (c) Image of tip following final thermal oxidation.

The thinned pillars can be sharpened into tips through a series of thermal oxidation procedures. At high temperatures in the presence of oxygen, silicon chemically reacts to form silicon dioxide. Approximately 46% of the resultant silicon oxide generated results from silicon consumed at the surface of the wafer while 54% is created from the ambient oxygen reacting with the surface[17].

When silicon is thermally oxidized stress builds up in regions of high curvature as a result of the specific volume difference between silicon and silicon dioxide. At temperatures below 1050˚C the viscosity of the silicon oxide is high enough that it cannot flow causing the stress to build. This stress build-up results in a suppression of the interfacial oxidation reaction, thereby slowing down the reaction in regions of high curvature. Since highest regions of curvature occur at the tips' base the oxidation reaction is occurring slower toward the base of the pillar than at the end, yielding a sharpened tip structure. At temperatures greater than 1050˚C the oxide viscosity reduces enough for the oxide to flow, relieving the stress build up that is required to slow down the reaction towards the base[16]. As a result all thermal oxidations for this study are conducted at 1000˚C.

The resulting silicon oxide is selectively etched in a buffered oxide solution consisting of 6:1 volume ratio of ammonium fluoride to hydrofluoric acid. The hydrofluoric acid consumes the silicon oxide while the ammonium fluoride stabilizes and controls uniformity of the reaction. Several iterations of thermal oxidation and etching are required to produce a sharp tip as seen in Figure 3.3c.

3.2 Cantilever Beam Formation

Cantilever beams are defined using photolithography and formed using an anisotropic dry etch. A 2.7μm thick negative photoresist, NR71-1500, is spun onto the wafer and then baked on a hotplate. The wafer is then loaded into the mask aligner and exposed to UV radiation using the beam formation mask [Figure 3.4]. The photoresist is developed and hard baked. The Bosch process is performed in the ICP-DRIE to etch the remainder of the device layer down to the buried oxide layer. The anchor and base regions defined during tip formation are also masked during beam formation. These regions have not been subjected to either anisotropic etch, however the HNA etching and thermal oxidation cycles have thinned them to approximately 4μm, four times the thickness of the beam which is approximately 1μm. This is important when considering the mechanical behavior of the device, since deflection is inversely related to the beam thickness cubed.

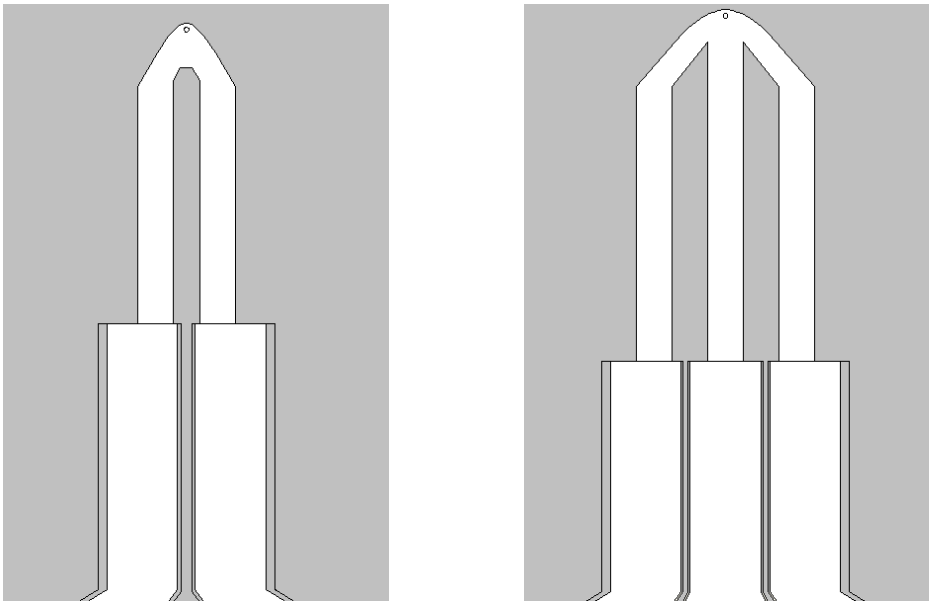
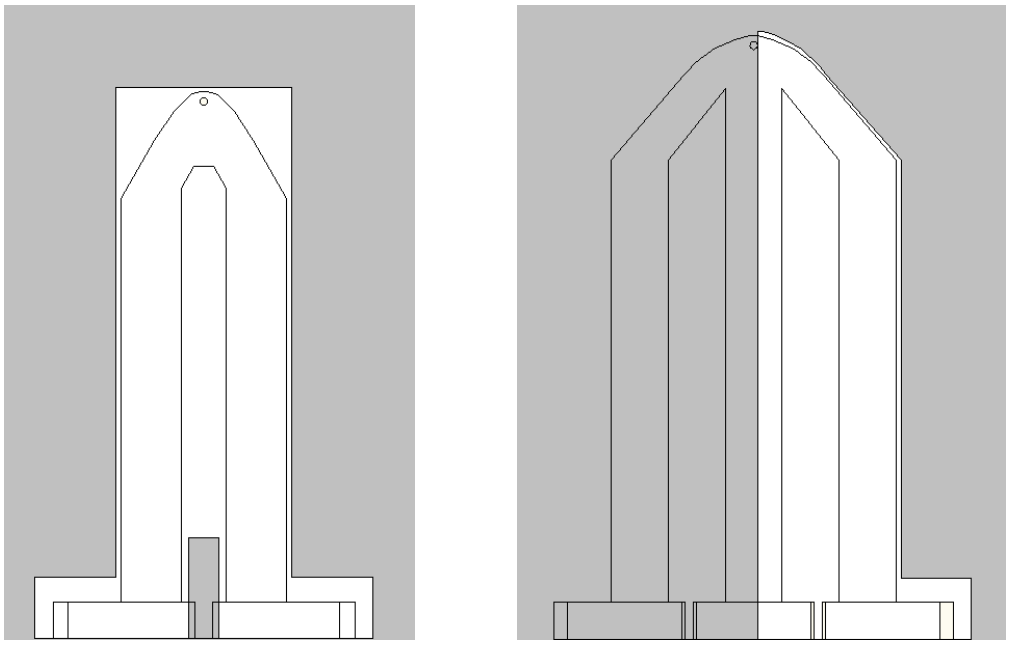


Figure 3.4 Beam Formation Mask. (a) Designs I, II (b) Designs III, IV, V, and VI. White areas represent where the cantilever beam will be formed. Shaded areas will be etched during anisotropic etching.

3.3 Electrical Activation

Cantilevers are made electrically active by doping the silicon in a series of ion implantations and diffusions. By implanting silicon with different impurity concentrations the number of charge carriers in regions can be controlled locally. This translates into the capability of controlling local resistivity and therefore resistance. High resistance regions release heat due to Joule heating when a current is passed. Joule heating phenomena can be realized by creating a current path primarily consisting of conductive high doped silicon with localized regions of low doped silicon which represent the heater region.

The low doping mask profiles for cantilevers I, II, III, and V are can be seen in Figure 3.5. Cantilevers IV and VI do not have heating elements and are completely masked with photoresist during the low dosage ion implantation. The thick photoresist layer prevents the masked portions of the wafer from being implanted. The two legged design the entire cantilever is selectively doped with the ion beam. For the three legged design only the right side is selectively doped such that a heater region will only exist between the center and right electrode. The intrinsic silicon has an intentionally high resistivity such that there is no current path travel between the right and left legs of the cantilever. This allows the three legged devices to sort material between the right and left electrodes without heating.



(a) **(b)**

Figure 3.5 Low Doping Mask. (a) Designs I, II (b) Designs III, V. White areas represent areas that will be exposed to the ion beam during low dosage implantation. Shaded areas indicate where the device will be masked with photoresist.

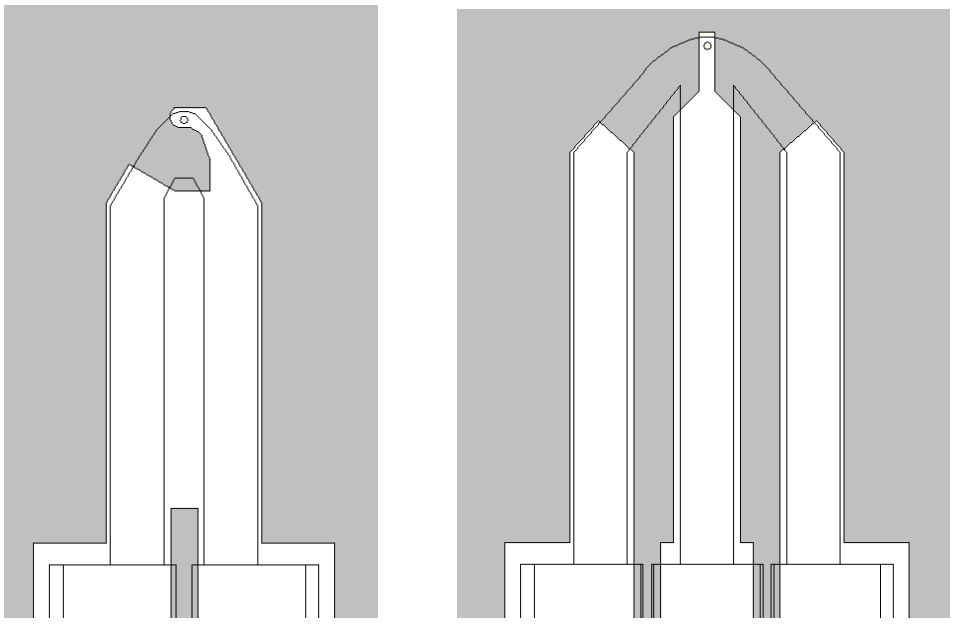
Areas to be exposed during ion implantation are defined using photolithography. To do this a 3μm layer of positive photoresist, Shipley 1827, is spun and exposed in the mask aligner using the low dosage mask in Figure 2.4. When positive photoresist is exposed to UV radiation the polymer chains in the resist scission, forming lower molecular weight fragments that become more soluble in an aqueous base solution yielding the desired pattern. The remaining photoresist is hard baked on and the wafers are shipped to Core Systems, an outside vendor, for ion implantation.

The low dosage implantation recipe creates a uniform background resistivity and will ultimately dominate the overall resistance of the device. Areas that are doped in the low dosage implantation step, but not doped during the high dosage implantation define the heater region. For the given design geometry an impurity concentration of 10^{17} atoms/cm^3 is desired. To achieve this impurity concentration a 200keV ion beam is used

to implant phosphorous ions onto the exposed surfaces of the wafer at a standard tilt angle of 7˚ leaving a surface concentration 2.51e13 atoms/cm^2. Following implantation the photoresist is stripped by soaking the wafer in acetone followed by a piranha clean and oxygen plasma is used to remove any remaining organic material. Annealing the wafer drives impurities from surface into the device thickness, resulting in the desired volumetric concentration. Since the diffusion of dopants is an isotropic process, an oxide layer is deposited to prevent out-diffusion of dopants from the wafer. A plasma enhanced chemical vapor deposition (PECVD) system is used to deposit 300nm of oxide on the wafer and a 0.5 hour diffusion is performed at 1000˚C in a nitrogen environment. Following diffusion the PECVD oxide layer is fully removed using buffered oxide etch bath.

The high doping mask profiles for all designs can be seen in Figure 3.6. For the two legged design the two legs are selectively doped up to the heater region. The right leg electrode also continues up the side of the cantilever to cover the tip, forming the tip electrode. A voltage potential can be placed between the tip electrode and a conductive substrate to deliver material during operation. The left leg is deliberately left short of the tip area forcing an applied current to travel through this region of higher resistance, which results in joule heating. Similarly, on the three legged design the center leg electrode covers the tip region to form the tip electrode. On the three legged design, both the left and right leg doping profiles are deliberately kept short of the heater region to ensure current would travel through the silicon only exposed to low dosage implantation. Since only the right side of the three legged devices were doped during the low dosage implantation step, there will only be heating when a voltage bias is placed between the

center and right electrode. On the contrary when a voltage bias is placed between the left and right, or the left and center electrode, no current will travel through the silicon. The thick photoresist layer prevents the masked portions of the wafer from being implanted.



(a) **(b)**

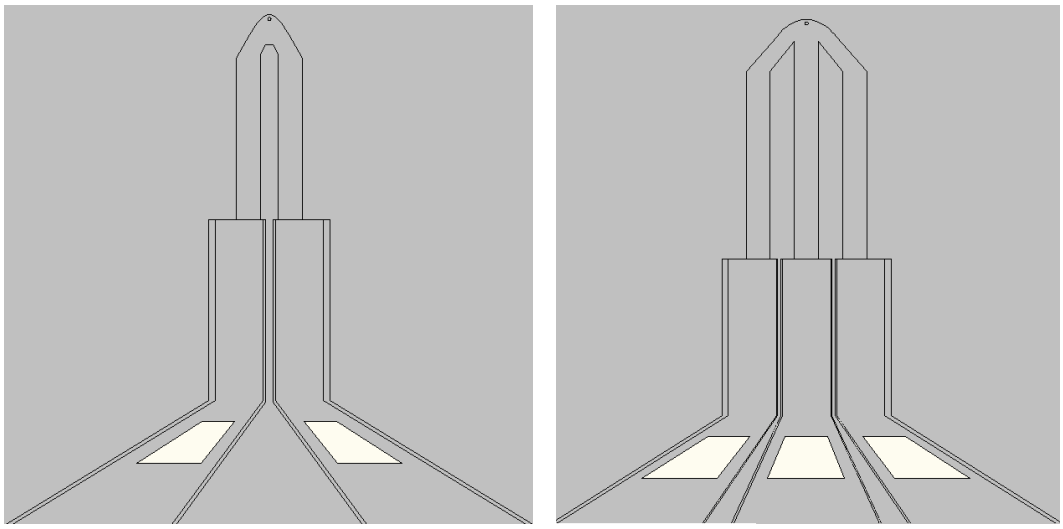
Figure 3.6 High Doping Mask. (a) Designs I, II (b) Designs III, IV, V, and VI. White areas represent areas that will be exposed to the ion beam during high dosage implantation. Shaded areas indicate where the device will be masked with photoresist.

Areas that will be exposed to high dosage ion implantation are defined using the same photolithography recipe as the low dosage implantation and can be seen in Figure 3.6. For the given design geometry an impurity concentration of 10^{20} atoms/cm^3 is desired. To achieve this impurity concentration a 200keV ion beam is used to implant phosphorous ions onto the exposed surfaces of the wafer at tilt angle of 45˚ and orientation of 180˚, leaving a surface concentration 2.51e16 atoms/cm^2. A tilt angle of 45˚ with an orientation of 180˚ is used to ensure there is an electrical path connecting the anchor to the leg; tilting the wafer ensures the sidewall connecting the two is doped. The high energy of the ion beam causes during implantation causes the wafer to heat up substantially. Following implantation photoresist is stripped by soaking the wafer in

acetone followed by a piranha clean and oxygen plasma is used to remove any remaining organic material. A 300nm PECVD oxide is deposited followed by a 2hr 1000˚C diffusion used to drive dopants into the thickness of the wafer. Following diffusion the PECVD oxide layer is fully removed using a buffered oxide etch bath.

3.4 Passivation & Metallization

Metallization of electro-thermal cantilevers is accomplished in three steps; 1) electrical passivation, 2) deposition and liftoff of contact electrodes, 3) deposition and liftoff of sorting electrodes. The passivation layer is used to keep the metal electrodes isolated from the now electrically active silicon layer. Small contact windows called vias are opened through the oxide layer. Controlling the regions where metal can contact silicon ensures current follows its desired path and obstructs current from leaking across the surface of the wafer which would short the device.. The contact electrode must be robust to cantilever deflections at the base of the cantilever beam, be resilient to abrasion during testing, and carry sufficient current to the device. The tip/sorting electrodes need to be thick enough to deliver sufficient current to heat the tip area while being thin enough to withstand bending along the cantilever beam length.

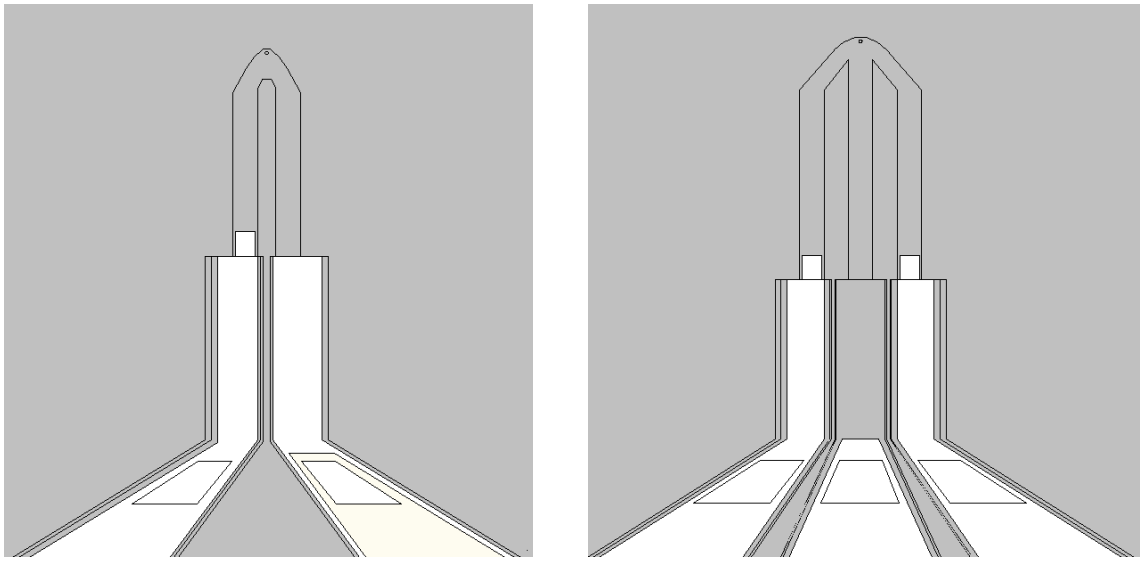


(a) **(b)**

Figure 3.7 Contact Vias Mask. (a) Designs I, II (b) Designs III, IV, V, and VI.
White areas represent areas that will be exposed during a reactive ion etch of the oxide layer. Shaded areas indicate where the device will be masked with photoresist such that the oxide layer remains.

A 50nm thick PECVD silicon oxide passivation layer is deposited onto the substrate. The oxide is patterned using a 3µm layer of positive photoresist, Shipley 1827 and exposed to the contact vias mask shown in Figure 3.7. Following photolithography, the exposed oxide is etched down to the silicon layer in a Freon (CF_4) process using a Reactive Ion Etching tool. Following reactive ion etching of the silicon oxide a BOE dip is performed to remove any oxide that may remain and the photoresist is stripped using acetone and piranha.

The wafer is patterned using the contact electrode mask shown in Figure 3.8 using positive photoresist, Shipley 1827. Following exposure in the mask aligner the wafer is developed and placed into the sputtering chamber where a 10nm chromium adhesion layer and 150nm gold contact layer are deposited onto the wafer. The metal is lifted off in acetone and sonicated to remove the metal sidewalls which result during sputter coating.



(a) **(b)**

Figure 3.8 Contact Electrode Mask. (a) Designs I, II (b) Designs III, IV, V, and VI. White areas represent areas that will be exposed during deposition of gold. Shaded areas indicate where the device will be masked with photoresist where the gold will be lifted off.

The wafer is patterned using the contact electrode mask shown in Figure 3.9 and placed into a buffered oxide etch solution to remove all of the oxide on the cantilever leg ensuring good contact between the beam electrode and highly doped silicon. A 100nm platinum layer is sputtered onto the wafer and lifted off in acetone. A 1 minute sonication is performed to remove free standing platinum flanges which result from photoresist sidewall coating. At this point the wafer can be tested with a multi-meter to sample device resistances values.

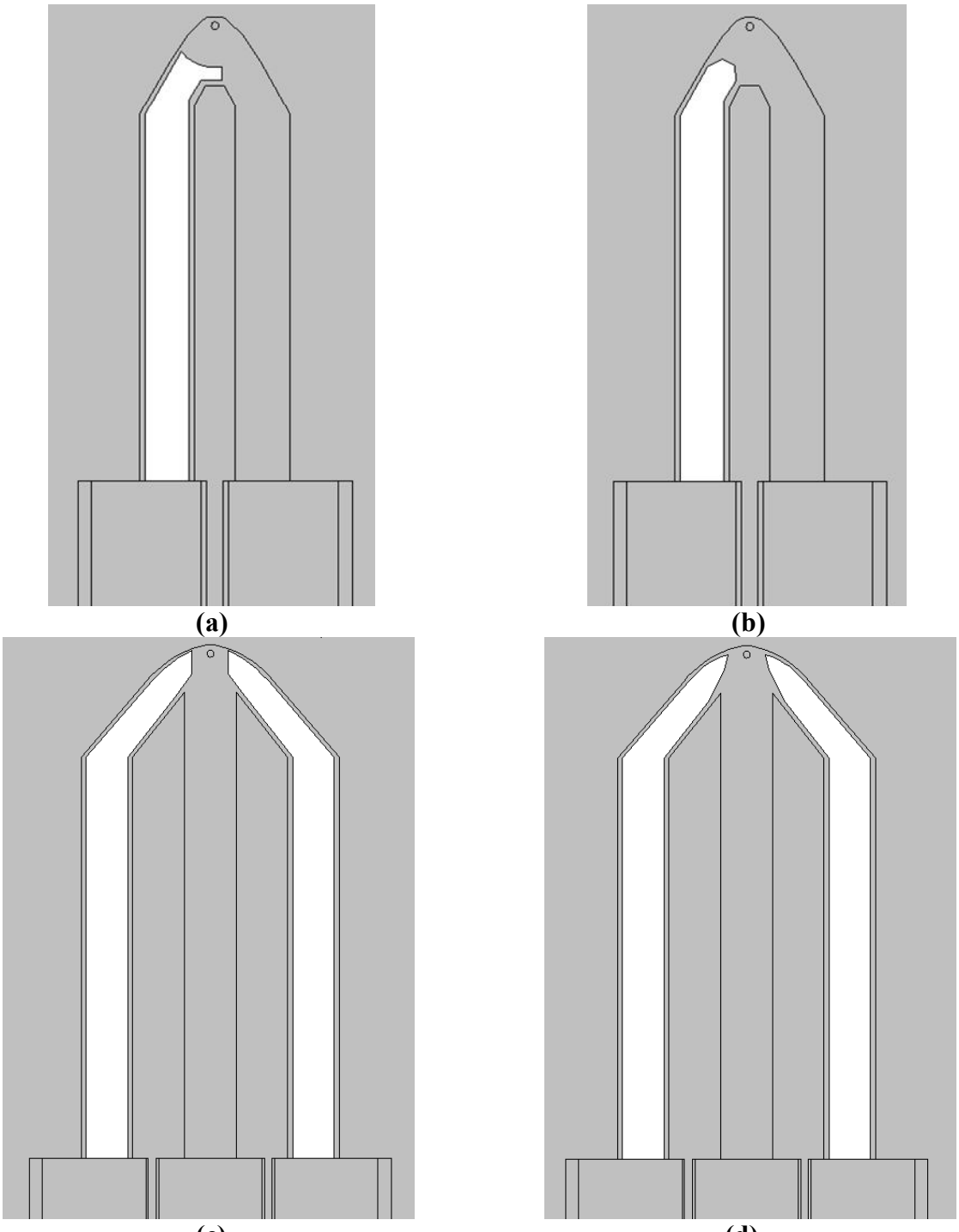
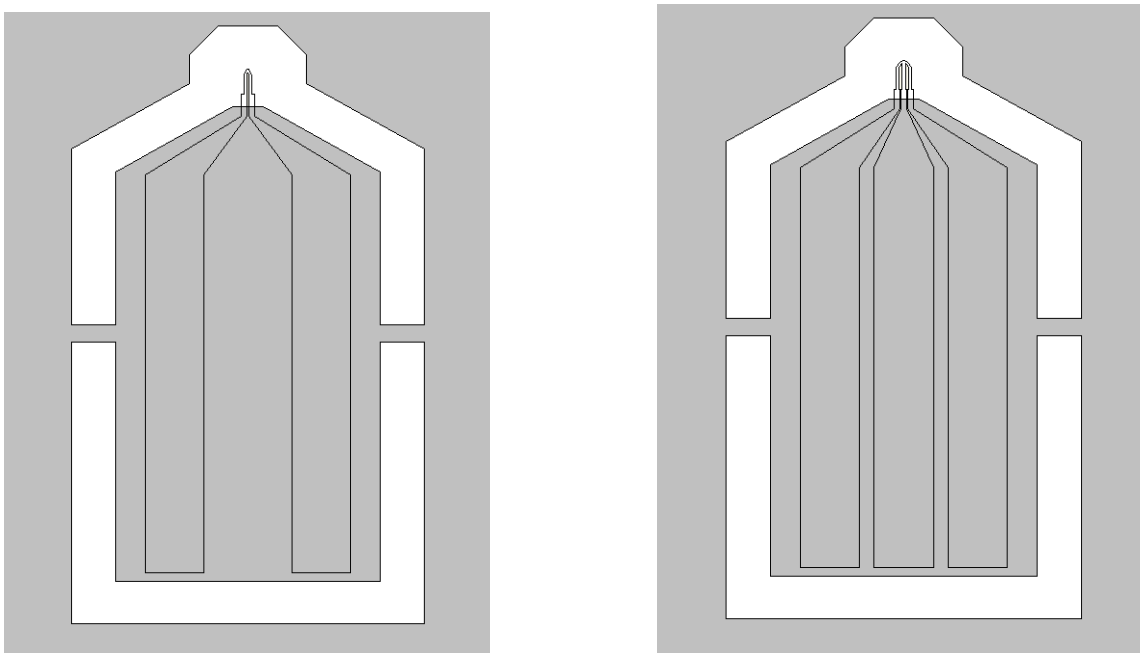


Figure 3.9 Beam Electrode Mask (a) Design I (b) Design II (c) Design III, IV (d) Design V, VI White areas represent regions that will be exposed during platinum deposition gold. Shaded areas indicate where the device will be masked with photoresist where the gold will be lifted off.

3.5 Device Release

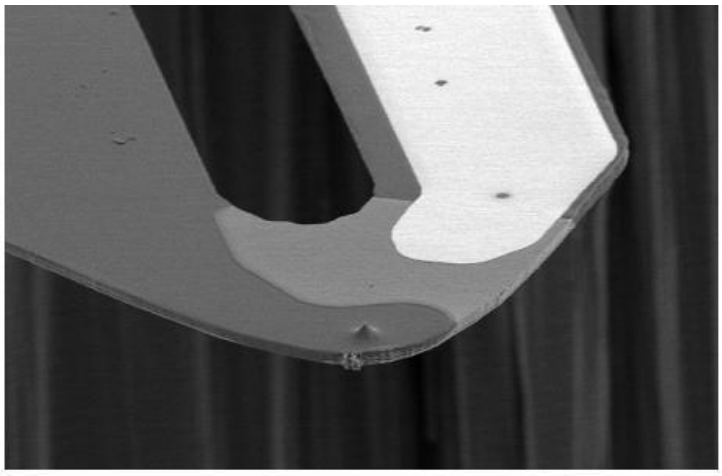
To produce free standing cantilevers, windows in the backside of the handle layer are anisotropically etched and the buried oxide layer is removed in a hydrofluoric acid bath. To protect the finished devices during the backside silicon etch, both a 300nm PECVD oxide and a 3μm layer of Shipley 1827 are deposited onto the topside of the wafer. Due to poor etch uniformity the ICP-DRIE, the wafer is diced with a scribe into four quadrants. Each wafer will undergo photolithography and backside etching independently. To do this a ~17μm thick negative photoresist, NR5-8000, is spun onto the backside of each quarter, exposed to the backside opening mask shown in Figure 3.10, developed and hard baked.



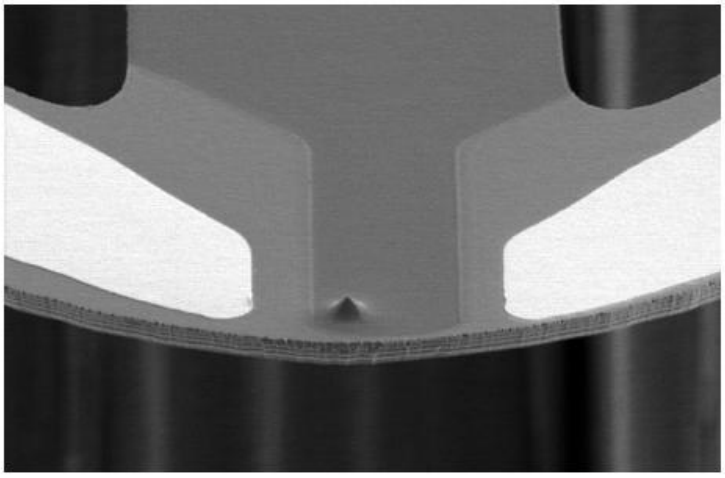
(a) **(b)**

Figure 3.10 Backside Opening Mask.(a) Designs I, II (b) Design III, IV, V, and VI. White areas represent windows that will be etched through the thickness of the handle layer. Shaded areas represent regions to be masked with photoresist during the backside etch.

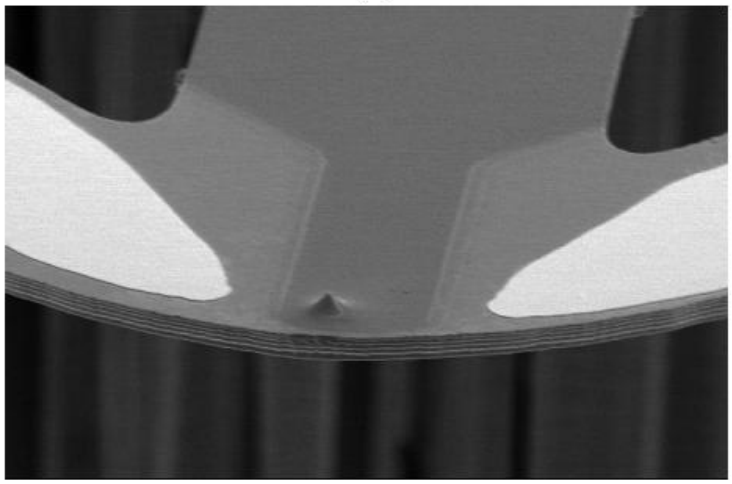
The quarter wafer is transferred onto a single side polished wafer that has been coated in thick photoresist and the two are cured together on a hotplate. The backside of the wafer is then etched in the Bosch process down to the buried oxide layer. The wafers are then placed into 1165 photoresist stripper overnight. The quarter wafer is removed from the carrier wafer and placed a piranha solution for 15 seconds to clean the wafer. A 40 second hydrofluoric acid bath consumes the buried oxide layer, fully releasing the cantilevers from the wafer. Devices can be punched out of the wafer, inspected, characterized, and utilized. SEM images of free standing devices are seen in Figure 3.10 and electrical properties for a Type II device are shown in Appendix B.



(a)



(b)



(c)

Figure 3.11. Released devices. (a) Type II (b) Type III, Type IV (c) Type V, Type VI

APPENDIX A

FABRICATION PROCESS FLOW TABLE

	Process Description	Material/Equipment	Recipe/Parameters
1	Wafer Parameters	100mm SOI <100>	N/Phosphorus 5µm - 1µm - 500µm ρ=38-52Ω·cm
2	Photoresist Spin Coating	High Speed Spinner BidTec SP-100	Dehydration bake: 150˚C, 5 min Spin Futurrex, NR71-1500 5000rpm - 1000rpm/s - 45s Soft bake: 150˚C, 1 min
3	Photolithography Mask #1 Tip Fabrication	Mask Aligner EV420 H-line (405 nm)	Hard contact, 40s exposure Post bake:100˚C, 1 min Develop in RD-6 12-15s Hard bake: 120˚C, 10 min
4	Anisotropic Topside Silicon Etch	ICP-DRIE Plasmatherm SLR 770	Bosch Process: 8-9 cycles
5	Etch Verification	Prolifometer Alpha Step IQ - 5µm tip	Expected etch depth 1.7-2.3µm
6	Remove Photoresist (PR)	Solvent/Acid Hood	Acetone soak: 10 min 10 min Piranha Solution (H2SO4:H2O :: 7:3) @120˚C
7	Device Inspection	Scanning Electron Microscope (SEM) Hitachi S4800	Verify tip pillar characteristics diameter ~2.7-3.5µm
8	Isotropic Silicon Etch	Acid Hood	Hydrofloric/Nitric/Acetic Acid (HNA) Bath 2%HF,3%CH3COOH,95%HNO3
9	Device Inspection	Scanning Electron Microscope (SEM) Hitachi S4800	Observe etch rate, etch in HNA until pillar diameter ~0.5µm
10	Oxidation Sharpen	Oxidation Furnace	Dry Oxidation, T=1000˚C, 15hrs O2 flow rate=6sccm
11	Silicon Dioxide Wet Etch	Acid Hood	Fully remove oxide in BOE (NH4F:HF::6:1) ~3.5min
12	Device Inspection	Scanning Electron Microscope (SEM) Hitachi S4800	Measure tip curvature, if blunt continue oxidation sharpening, usually ~3 iterations

13	Photoresist Spin Coating	High Speed Spinner BidTec SP-100	Dehydration bake: 150˚C, 5 min Spin Futurrex, NR71-1500 1000rpm - 200rpm/s - 45s Soft bake: 150˚C, 1.5 min
14	Photolithography Mask #2 Cantilever Beam Formatoin	Mask Aligner EV420 H-line (405 nm)	Hard contact, 25s exposure Post bake:100˚C, 1 min Develop in RD-6 ~40s Hard bake: 120˚C, 10 min
15	Anisotropic Topside Silicon Etch	ICP-DRIE Plasmatherm SLR 770	Bosch Process: 10-12 cycles
16	Etch Verification	Optical Microscope	Verify etch depth has reached box oxide
17	Remove Photoresist (PR)	Solvent/Acid Hood	Acetone soak: 10 min 10 min Piranha Solution (H2SO4:H2O :: 7:3) @120˚C
18	Photoresist Spin Coating	High Speed Spinner BidTec SP-100	Dehydration bake: 150˚C, 5 min Spin Shipley 1827 3000rpm - 300rpm/s - 45s Soft bake: 120˚C, 1.5 min
19	Photolithography Mask #3 Low Dose Implantation	Mask Aligner EV420 H-line (405 nm)	Hard contact, 20s exposure Develop in MF319 ~55s Hard bake: 120˚C, 25 min
20	Ion Implantation	Outside Vendor CORE systems, CA	N/Phosphorus 2.51E13atoms/cm2 200keV/ 7˚ tilt
21	Remove Photoresist (PR)	Solvent/Acid Hood RIE - March Jupiter III	Acetone soak: 10 min 10 min Piranha Solution (H2SO4:H2O :: 7:3) @ 120˚C 5 min O2 plasma, 300W
22	Oxide Deposition	Plasmalab PECVD	Deposition Thickness: 300nm 12 min high power
23	Dopant Diffusion	Annealing Furnace	1000˚C, 30 min N2 flow = 2 sccm
24	Silicon Dioxide Wet Etch	Acid Hood	Fully remove oxide in BOE (NH4F:HF::6:1) ~4min, until Si is hydrophobic
25	Photoresist Spin Coating	High Speed Spinner BidTec SP-100	Dehydration bake: 150˚C, 5 min Spin Shipley 1827 3000rpm - 300rpm/s - 45s Soft bake: 120˚C, 1.5 min

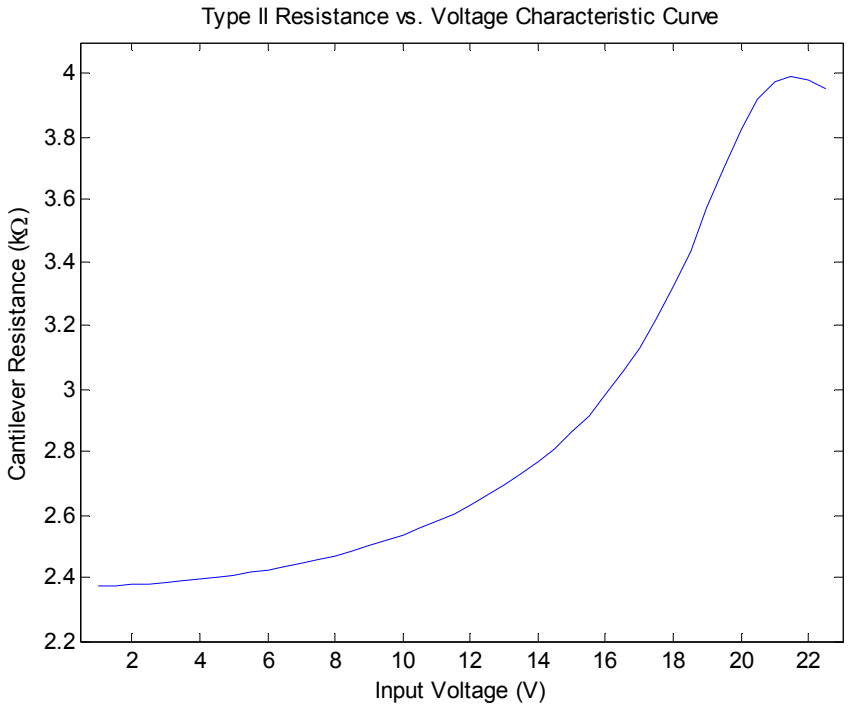
26	Photolithography Mask #4 High Dose Implantation	Mask Aligner EV420 H-line (405 nm)	Hard contact, 20s exposure Develop in MF319 ~55s Hard bake: 120˚C, 25 min
27	Ion Implantation	Outside Vendor CORE systems, CA	N/Phosphorus 2.51E16atoms/cm2 200keV/ 45˚ tilt/180˚ Orientation
28	Remove Photoresist (PR)	Solvent/Acid Hood RIE Axic	Acetone soak: overnight & 1 min in ultrasound 10 min Piranha Solution 5 min O2 plasma, 500W
29	Oxide Deposition	Plasmalab PECVD	Deposition Thickness: 300nm 12 min high power
30	Dopant Diffusion	Annealing Furnace	1000˚C, 2 hrs N2 flow = 2 sccm
31	Silicon Dioxide Wet Etch	Acid Hood	Fully remove oxide in BOE (NH4F:HF::6:1) ~4min, until Si is hydrophobic
32	Oxide Deposition	Plasmalab PECVD	Deposition Thickness: 50nm
33	Photoresist Spin Coating	High Speed Spinner BidTec SP-100	Dehydration bake: 150˚C, 5 min Spin Shipley 1827 3000rpm - 300rpm/s - 45s Soft bake: 120˚C, 1.5 min
34	Photolithography Mask #5 Contact Vias	Mask Aligner EV420 H-line (405 nm)	Hard contact, 20s exposure Develop in MF319 ~55s Hard bake: 120˚C, 25 min
35	Isotropic Topside Silicon Etch	Freon RIE	Etch 300nm with CF4 plasma
36	Silicon Dioxide Wet Etch	Acid Hood	Remove any remaining oxide in BOE (NH4F:HF::6:1) ~0.5min
37	Remove Photoresist (PR)	Solvent/Acid Hood RIE Axic	Acetone soak: 10min Piranha Solution: 10min
38	Photoresist Spin Coating	High Speed Spinner BidTec SP-100	Dehydration bake: 150˚C, 5 min Spin Shipley 1827 3000rpm - 300rpm/s - 45s Soft bake: 120˚C, 1.5 min

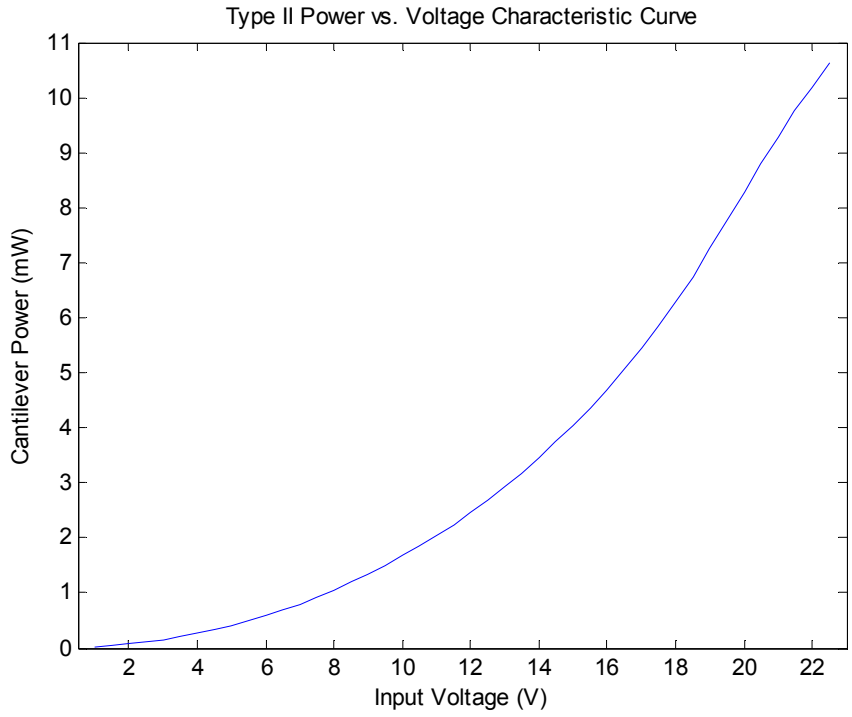
39	Photolithography Mask #6 Contact Electrodes	Mask Aligner EV420 H-line (405 nm)	Hard contact, 20s exposure Develop in MF319 ~55s
40	Metal Deposition	Sputterer - Metals - AJA	Deposit 10nm Cr adhesion layer Deposit 150nm Au layer
41	Lift Off	Solvent Hood	Soak in acetone overnight Sonicate for 1 min to remove sidewalls
42	Device Inspection	Multimeter	Test device resistance
43	Photoresist Spin Coating	High Speed Spinner BidTec SP-100	Dehydration bake: 150˚C, 5 min Spin Shipley 1827 3000rpm - 300rpm/s - 45s Soft bake: 120˚C, 1.5 min
44	Photolithography Mask # 7 Beam Electrode	Mask Aligner EV420 H-line (405 nm)	Hard contact, 20s exposure Develop in MF319 ~55s
45	Silicon Dioxide Wet Etch	Acid Bench	Remove any remaining oxide on unmasked portion with BOE ~1min
46	Metal Deposition	Sputterer - Metals - AJA	Deposit 100nm Pt
47	Lift Off	Solvent Hood	Soak in acetone overnight Sonicate for 1 min to remove sidewalls
48	Oxide Deposition	Plasmalab PECVD	Deposition Thickness: 300nm 12 min high power
49	Photoresist Spin Coating	High Speed Spinner BidTec SP-100	Dehydration bake: 150˚C, 5 min Spin Shipley 1827 3000rpm - 300rpm/s - 45s Soft bake: 120˚C, 1.5 min Hard bake: 110˚C, 10min
50	Wafer Cleaving	Work Bench with Diamond Scribe	Cleave wafer into 4 quadrants
51	Photoresist Spin Coating	High Speed Spinner BidTec SP-100	Dehydration bake: 150˚C, 5 min Spin Futurrex, NR5-8000 1000rpm - 200rpm/s - 40s Soft bake: 150˚C, 6 min

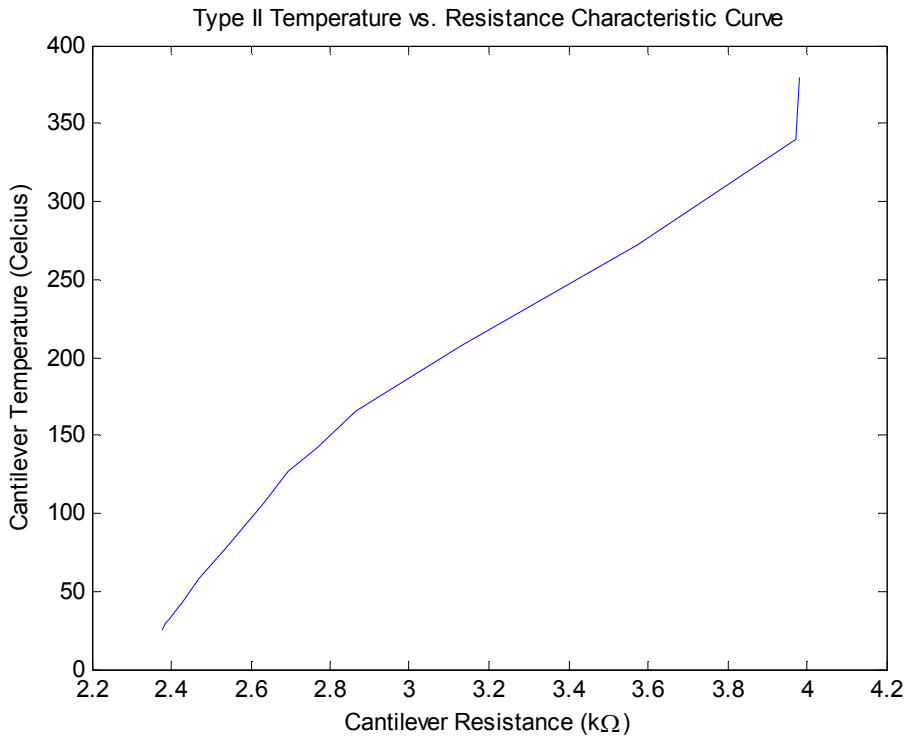
52	Photolithography Mask # 7 Beam Electrode	Mask Aligner EV420 H-line (405 nm)	Backside Alignment Hard contact, 30s exposure Develop in RD6 ~70s Hard bake: 120˚C, 10 min
53	Mount Quarter Wafer on Carrier Wafer	Spinner Hood Carrier Wafer: Single Side Polished Silicon	Dehydration bake: 150˚C, 5 min Spin Futurrex, NR5-8000 1000rpm - 200rpm/s - 40s Attach quarter wafer to carrier Hard bake: 120, 35 min
54	Backside Silicon Anisotropic Etch	ICP-DRIE Plasmatherm SLR 770	Bosch Process 500µm etch 900-1000 cycles Inspect w/ optical microscope
55	Separate Wafers	Solvent Hood	PR Stripper 1165, overnight
56	Wafer Clean	Acid Bench	Piranha @120˚C 15sec
57	Device Release	Acid Bench	HF 49%, 30-40s
58	Final Check	Scanning Electron Microscope (SEM) Hitachi S4800	Inspect final condition of cantilevers

APPENDIX B

THERMAL CANTILEVER CHARACTERISTICS






Type II Temperature vs. Resistance Characteristic Curve
Cantilever Temperature (Celcius)
Cantilever Resistance (kΩ)
0
50
100
150
200
250
300
350
400
2.2
2.4
2.6
2.8
3
3.2
3.4
3.6
3.8
4
4.2

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